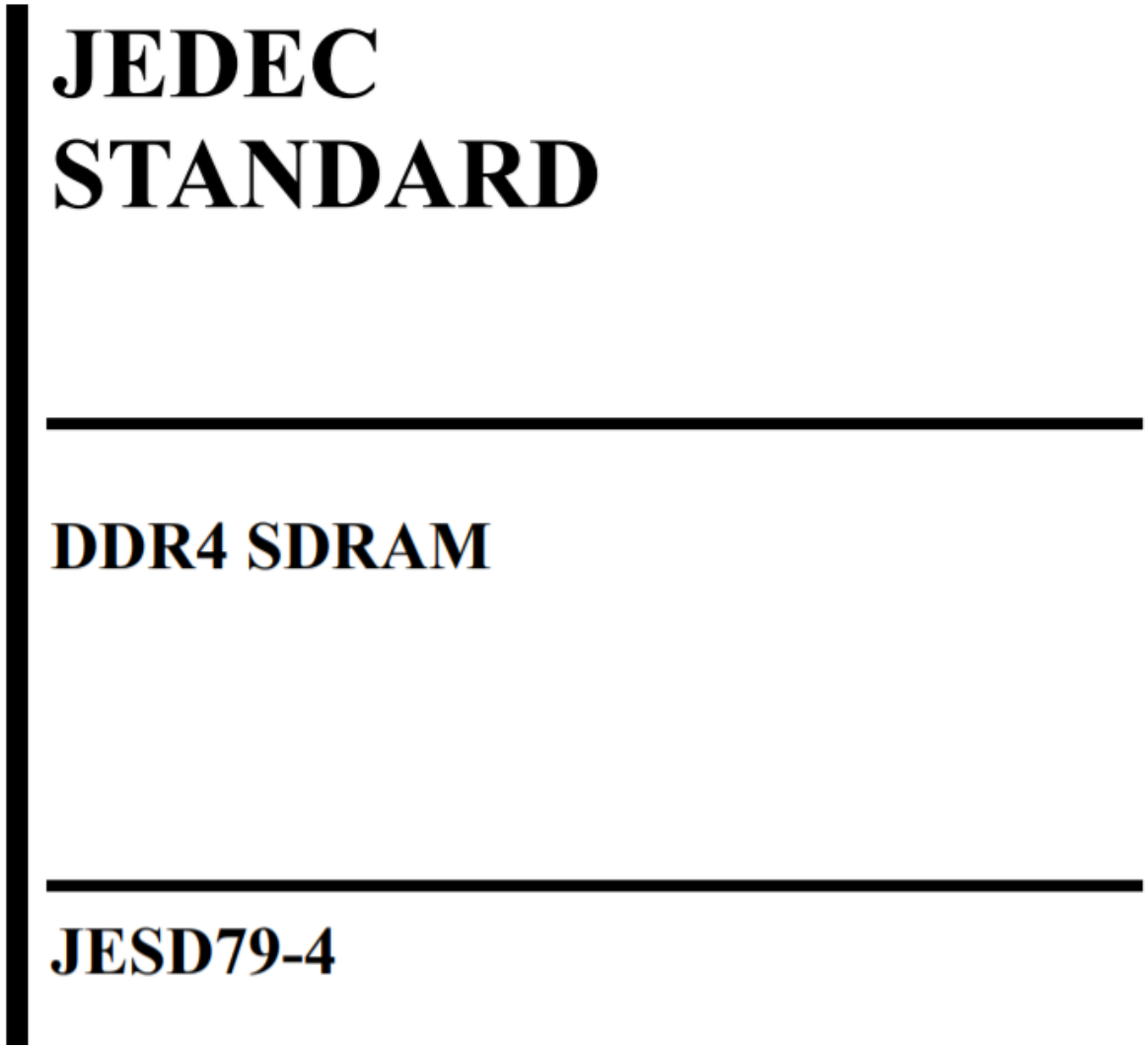
EXHIBIT B

US6603330	Radisys DCEngine 16U System (“The Accused Product”)
25. A method of programming a programmable digital circuit block, comprising the steps of:	The accused product discloses a method of programming a programmable digital circuit block (e.g., DDR 4 SDRAM). DCEngine 16U System Hyperscale Infrastructure for Communication Service Providers The new DCEngine framework transforms service provider central offices into SDN-enabled virtualized data centers. DCEngine provides a multi-rack level network functions virtualization (NFVi) and container based infrastructure for hosting thousands of virtualized network functions (VNFs) and applications under open software-defined networking (SDN) control. Service providers use DCEngine to provide pools of compute and storage resources that they can quickly scale to meet their evolving service requirements while improving agility in their service delivery. DCEngine utilizes the principles of highly efficient open compute platform (OCP) architectures and integrates fully supported open source software. Radisys designed DCEngine to address telco central office demands for seismic, power, emissions and NEBS, which are above and beyond the traditional data center requirements. Radisys' wealth of telecom platform expertise, along with 25+ years of experience providing telecom professional services, makes us the ideal partner for service providers transitioning to the hyperscale data center. DCEngine 16U System Highlights • 16U Integrated Rack designed for power, space, and weight limited deployments • Up to 10 shelves (2U each), configurable with Compute Sleds or Storage Sleds depending on your SDN or NFV application requirements • Configurable up to 1.2 Petabytes of storage • Configurable up to 48 Intel® Xeon® processors • Radisys Professional Services can also pre-integrate your required open source or commercial host OS, hypervisor, container, platform and / or orchestration software • Recommended platform for Central Office Re-architected as a Datacenter (CORD) Proof-of-Concept (PoC) deployments Component Overview  • Top of Rack 32 QSFP28 100GbE ports (32x40GbE, or 128 10/25GbE capable ports)  • Compute Sled 2U half wide rear view (top opened) showing blind mate connector  • Storage Sled 2U full width rear view (top opened) showing blind mate connector  https://hub.radisys.com/i/902083-dcengine-16u-system/0

Configuration Specifications

CONFIGURATION		DC-ENGINE FEATURES
Rack Configurations	Dimensions	16U Telco rack 1000mm depth, 600mm width
	Power	1U power conversion shelf, with 4 PSU bays, each rated at 2500W, 90-264VAC Input
	Dataplane Switch	1U (1 or 2), 32x 40GbE, or 128 10/25GbE for network traffic
	M anagement Switch	1U (1) Management / IPMI switches, 48 SFP+ 1/10GbE, 6 QSFP+ 40GbE Ports (up to 72 10Gbe available ports)
	Payload Shelves	Frame supports up to 6 x 2U shelves, selectable for server or storage sleds
	Compute Shelf	2U shelf holds to 2 x 2U half wide server sleds
	Storage Shelf	2U full width carrier
Compute Sled	Server Board	Dual socket Intel Server Board
	Configuration	Each half width sled supports 2 server boards, each server has 2 CPU sockets
	CPU	2 x Intel E5-26xx processors per server board to suit specific deployment power limits
	RAM	8 DIMM sockets per processor. DDR4 288-pin PC4-2133, 1.2V with ECC, up to 512GB / sled
	Storage	2 x 2TB 2.5" SSD plus 1 x M.2 for boot / OS per server board
	NIC (per server)	Dual 10 / 25G NICs (data) 1GbE IPMI interface per server.

https://hub.radisys.com/i/902083-dcengine-16u-system/1

	 Source: DDR 4 standard
a) loading a plurality of	The accused product discloses loading a plurality of configuration data (e.g., bits A1, A0) corresponding to any one of

configuration data corresponding to any one of a plurality of predetermined digital functions into a configuration register of said programmable digital circuit block; and	a plurality of predetermined digital functions (e.g., read/write operations of fixed burst length of BC8 or BC4; read/write operations of on-the-fly burst length of BC8 or BC4) into a configuration register (e.g., Mode register MR0) of said programmable digital circuit block (e.g., DDR 4 SDRAM). 3.4.1 Programming the mode registers For application flexibility, various functions, features, and modes are programmable in seven Mode Registers, provided by the DDR4 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. The mode registers are divided into various fields depending on the functionality and/or modes. As not all the Mode Registers (MR#) have default values defined, contents of Mode Registers must be initialized and/or re-initialized, i. e. written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array Source: DDR 4 standard

3.5 Mode Register

MR0

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	RFU	0 = must be programmed to 0 during MRS
A11:A9	WR and RTP[2, 3]	Write Recovery and Read to Precharge for auto precharge(see Table 1)
A8	DLL Reset	0 = NO 1 = Yes
A7	TM	0 = Normal 1 = Test
A6:A4,A2	CAS Latency[4]	(see Table 2)

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Address	Operating Mode	Description
A3	Read Burst Type	0 = Sequential 1 = Interleave
A1:A0	Burst Length	00 = 8 (Fixed) 01 = BC4 or 8 (on the fly) 10 = BC4 (Fixed) 11 = Reserved

Source: DDR 4 standard

b) configuring said programmable digital circuit block to perform any one of said plurality of predetermined digital functions based on said configuration data, wherein said steps a) and b) are dynamically performed, and wherein said programmable digital circuit block includes a data register for storing data to facilitate performing any one of said plurality of predetermined digital functions.	The accused product discloses configuring said programmable digital circuit block (e.g., DDR 4 SDRAM) to perform any one of said plurality of predetermined digital functions (e.g., read/write operations of fixed burst length of BC8 or BC4; read/write operations of on-the-fly burst length of BC8 or BC4) based on said configuration data (e.g., bits A1, A0), wherein said steps a) and b) are dynamically performed (e.g., on-the-fly BC is dynamically performed based on MRS command), and wherein said programmable digital circuit block includes a data register (e.g., register storing) for storing data to facilitate performing any one of said plurality of predetermined digital functions. The data is bit A12. It is used according to the configuration data MR0 [A1, A0] to facilitate performing any one of the predetermined digital functions. For instance, if MR0[A1, A0] indicates on-the-fly (OTF) burst length, then A12 determines if the OTF burst length is BC4 or 8, and hence facilitates performing the read/write operations of OTF burst length BC4 or 8. 3.4.1 Programming the mode registers For application flexibility, various functions, features, and modes are programmable in seven Mode Registers, provided by the DDR4 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. The mode registers are divided into various fields depending on the functionality and/or modes. As not all the Mode Registers (MR#) have default values defined, contents of Mode Registers must be initialized and/or re-initialized, i. e. written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array Source: DDR 4 standard

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A13	RFU	0 = must be programmed to 0 during MRS
A12	RFU	0 = must be programmed to 0 during MRS
A11:A9	WR and RTP[2, 3]	Write Recovery and Read to Precharge for auto precharge(see Table 1)
A8	DLL Reset	0 = NO 1 = Yes
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Source: DDR 4 standard

Table 16 — Command Truth Table

Function	Abbreviation	CKE		CS_n	ACT_n	RAS_n /A16	CAS_n /A15	WE_n/ A14	BG0-BG1	BA0-BA1	C2-C0	A12/ BC_n	A17, A13, A11	A10/ AP	A0-A9	NOTE
		Previous Cycle	Current Cycle													
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V	OP Code				12
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	7,9
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	7,8,9, 10
				L	H	H	H	H	V	V	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	L	V	
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	H	V	
RFU	RFU	H	H	L	H	L	H	H	RFU							
Bank Activate	ACT	H	H	L	L	Row Address(RA)			BG	BA	V	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	6
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	6
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	V	H	V	
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	L	V	

Source: DDR 4 standard

A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.

Source: DDR 4 standard

In the same manner that on-the-fly Burst Chop is configured and executed dynamically, the MRS can also be configured to dynamically execute on-the fly refresh rates as shown below.

4.9.1 Mode Register and Command Truth Table

The Refresh cycle time (tRFC) and the average Refresh interval (tREFI) of DDR4 SDRAM can be programmed by MRS command. The appropriate setting in the mode register will set a single set of Refresh cycle time and average Refresh interval for the DDR4 SDRAM device (fixed mode), or allow the dynamic selection of one of two sets of Refresh cycle time and average Refresh interval for the DDR4 SDRAM device(on-the-fly mode). The on-the-fly mode must be enabled by MRS as shown in Table 21 before any on-the-fly- Refresh command can be issued.

Table 21 — MR3 definition for Fine Granularity Refresh Mode

A8	A7	A6	Fine Granularity Refresh
0	0	0	Normal mode (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Enable on the fly 2x
1	1	0	Enable on the fly 4x
1	1	1	Reserved

There are two types of on-the-fly modes (1x/2x and 1x/4x modes) that are selectable by programming the appropriate values into the mode register. When either of the two on-the-fly modes is selected ('A8=1'), DDR4 SDRAM evaluates BG0 bit when a Refresh command is issued, and depending on the status of BG0, it dynamically switches its internal Refresh configuration between 1x and 2x (or 1x and 4x) modes, and executes the corresponding Refresh operation. The command truth table is as shown in Table 22.

Source: DDR 4 standard

Table 22 — Refresh command truth table

Function	CS_n	ACT_n	RAS_n /A15	CAS_n /A14	WE_n /A13	BG1	BG0	BA0-1	A10/ AP	A0-9, A11-12, A16-20	MR3 Setting
Refresh (Fixed rate)	L	H	L	L	H	V	V	V	V	V	A8 = '0'
Refresh (on-the-fly 1x)	L	H	L	L	H	V	L	V	V	V	A8 = '1'
Refresh (on-the-fly 2x)	L	H	L	L	H	V	H	V	V	V	A8:A7:A6='101'
Refresh (on-the-fly 4x)											A8:A7:A6='110'

Source: DDR 4 standard